IN THE CLAIMS:

Please delete the paragraph heading on page 8 of the English translation of the subject application, line 1, and insert in place thereof the paragraph heading as follows:

--CLAIMS--

Please insert the paragraph heading on page 8 of the English translation of the subject application, before claim 1, the following:

-- What is claimed is: --.

Please amend claims 1-5 as follows:

1. (Amended) A circuit for generating an asynchronous signal pulse having a predetermined duration at an output of an integrated circuit, which has

a first and a second transistor in the integrated circuit, which are connected in series between a supply potential (UDD) and ground (GND), firstly a control pulse having the predetermined duration being present at a control connection of the first transistor and then a control pulse being present at a control connection of the second transistor, with the result that, for the predetermined duration, firstly the first transistor and then the second transistor is turned on and the connecting point is firstly at the supply potential (UDD) and then at the ground (GND), and

a resistor for the definition of the active signal state, which is connected outside the integrated circuit in parallel with one of the two transistors in the integrated circuit either between the supply potential (UDD) and the connecting point or between the ground (GND) and the connecting point.

2. (Amended) The circuit as claimed in claim 1, wherein a waiting time (Δt) is provided between the first control pulse and the second control pulse, in which the two pulses do not overlap.

3. (Amended) The circuit as claimed in claim 2, wherein one of the two control pulses is generated from the other of the two control pulses by an inverter delay device.

4. (Amended) The circuit as claimed in claim 1, wherein the first transistor is a P-channel MOS transistor and the second transistor is an N-channel MOS transistor, the control connection of the first transistor being inverted.

5. (Amended) The circuit as claimed in claim 4, wherein the first transistor and the second transistor form a CMOS inverter with independent control gate connections.

REMARKS

The amendments to the specification as set forth above are intended to clarify and set apart the various sections of the subject application.

The amendments to the claims as set forth above are intended to remove all multiple dependent claims from the subject application and to more particularly point out and distinctly claim the subject invention.